IN THE SPECIFICATION:

Please replace paragraph 0007 of the specification with the following amended paragraph.

One embodiment of the present invention provides a Phase-Locked Loop with multiphase clocks. The Phase-Locked Loop includes a main loop, a calibration loop, and a ~~Multiplexer~~ Demultiplexer. The main loop includes, coupled in series, a Phase Frequency Detector, a Main Charge Pump, a Main Loop Filter, a Multi-Phase Voltage Controlled Oscillator and a Phase-switching Fractional Divider. The calibration loop includes Y Calibration Loop Filters, with Y being an integer, coupled to the Multi-Phase Voltage Controlled Oscillator, and Control Logic for controlling the Phase-Switching Fractional Divider. The ~~Multiplexer~~ Demultiplexer is coupled between an output of the Main Charge Pump and inputs of the Main Loop Filter and the Y Calibration Loop Filters. A Reference Frequency Signal is coupled to the Phase Frequency Detector, a control signal from the Control Logic is coupled to the ~~Multiplexer~~ Demultiplexer, and a Calibration Signal is coupled to a control input of the Control Logic.

Please replace paragraphs 0016 to 0020 of the specification with the following amended paragraphs.

The prior art solution is depicted in Fig.1. As shown, a first (Main) loop comprises, coupled in cascade, a Phase Frequency Detector (PFD) 1, a Main Charge Pump 2, a Main Loop Filter 3, a Multi-Phase Voltage Controlled Oscillator (VCO) 4 and a Phase-switching Fractional Divider 5. A second (Calibration) loop comprises the series connection of a Calibration Charge Pump 9, a ~~Multiplexer~~ Demultiplexer 6 and Y Calibration Loop Filters 7, with Y being an integer, coupled between the Phase Frequency Detector (PFD) 1 and the Multi-Phase Voltage Controlled Oscillator (VCO) 4. The ~~Multiplexer~~ Demultiplexer 6 is controlled by Control Logic 8 coupled to the Phase-Switching Fractional Divider 5. A Reference Frequency Signal 10 is applied to the Phase Frequency Detector 1. The Calibration signal 11 is applied to a control input of the Control Logic 8.

Fig. 2 represents one embodiment of the present invention. In this device, the control logic 8 controls the ~~multiplexer~~ demultiplexer 6 in such a way that most of the time the main loop filter is chosen and sometimes one of the calibration loop filters is chosen. Most of the

cycles of this charge pump are indeed used for the main loop, which has the highest bandwidth. In this state, ~~multiplexer~~ demultiplexer 6 is just a through connection. However, from time to time, a cycle of the charge pump current is taken from the main loop and used for the calibration loop. When this occurs, the ~~multiplexer~~ demultiplexer 6 guides the current towards one of the filters 7. Which filter exactly is chosen is determined by the state that the phase-switching fractional divider is in.

Fig. 2 shows the two loops in the system. A first (Main) loop comprises, coupled in cascade, a Phase Frequency Detector (PFD) 1, a Main Charge Pump 2, a Main Loop Filter 3, a Multi-Phase Voltage Controlled Oscillator (VCO) 4 and a Phase-switching Fractional Divider 5. A second loop (Calibration) comprises the series connection of a ~~Multiplexer~~ Demultiplexer 6 and Y Calibration Loop Filters 7, with Y being an integer, coupled between the Phase Frequency Detector (PFD) 1 and the Multi-Phase Voltage Controlled Oscillator (VCO) 4. The ~~multiplexer~~ demultiplexer 6 is controlled by Control Logic 8 coupled to the Phase-Switching Fractional Divider 5, and a Reference Frequency Signal 10 is applied to the Phase Frequency Detector 1.

The ~~multiplexer~~ demultiplexer 6 has an input connected to an output of the Main Charge Pump 2, and has outputs connected to inputs of the Main Loop Filter 3 and of Y Calibration Loop Filters 7. The Calibration signal 11 is applied to a control input of the Control Logic 8.

A practical example might be that, for Y=8, one out of nine cycles is used for calibration.

- Suppose we want to divide by N+1/8. In this case the phase switching divider output is subsequently aligned with phase 1-2-3-4-5-6-7-8-1-2-3-4- and so on. Therefore, the ~~multiplexer~~ demultiplexer sequence shown in the left side of the table below can be used, where M denotes the main loop and Cx calibration loop x, with x = 1 to 8.
- Suppose we want to obtain a division by N+2/8. Then the phase switching divider output is subsequently aligned with phase 1-3-5-7-1-3-5-7-1-3- and so on. This leads to the ~~multiplexer~~ demultiplexer sequence shown in the right side of the table below.

Please delete the paragraph beginning at page 14, line 2 of the specification (abstract).

Please replace the paragraph beginning at page 14, line 4 of the specification (abstract) with the following amended paragraph.

A Phase-Locked Loop with multiphase clocks is provided. The Phase-Locked Loop includes a main loop, a calibration loop, and a ~~Multiplexer~~ Demultiplexer. The main loop includes, coupled in series, a Phase Frequency Detector, a Main Charge Pump, a Main Loop Filter, a Multi-Phase Voltage Controlled Oscillator and a Phase-switching Fractional Divider. The calibration loop includes Y Calibration Loop Filters, with Y being an integer, coupled to the Multi-Phase Voltage Controlled Oscillator, and Control Logic for controlling the Phase-Switching Fractional Divider. The ~~Multiplexer~~ Demultiplexer is coupled between an output of the Main Charge Pump and inputs of the Main Loop Filter and the Y Calibration Loop Filters. A Reference Frequency Signal is coupled to the Phase Frequency Detector, a control signal from the Control Logic is coupled to the ~~Multiplexer~~ Demultiplexer, and a Calibration Signal is coupled to a control input of the Control Logic.